Degree Examination in EG40GD Communications Engineering 2

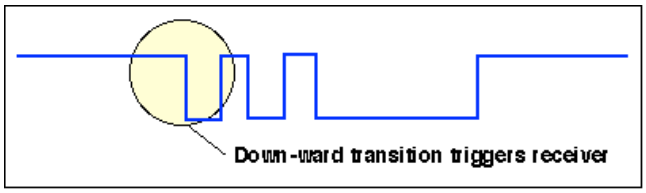
Candidates must answer FOUR questions.
– All questions carry 25 marks

Q Marks

1.

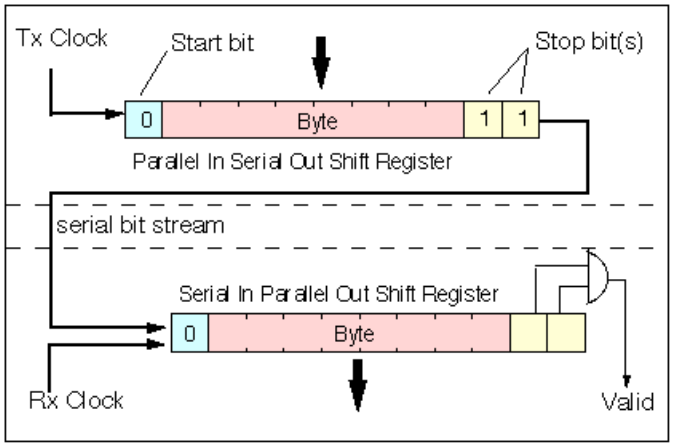
1(a) 8 e DMX-512 bus uses ***asynchronous character framing***. Sketch the signal waveform that is received when the value 0x0E was sent.

The answer must identify the asynchronous framing. Slots are sent using an RS-485 line signal and asynchronous character framing.



Identification of the start of a frame

There is an arbitrary idle gap between slots, identified by a Mark level (high) The bits in a byte are sent LSB first, using a shift register. Each slot starts with one start bit (low), followed by the data byte and each valid slot ends with two stop bits (high). The start of each slot is therefore identified by the receiver by a downwards (space) transition in the received line voltage. This triggers reception of the 11-bit slot using a shift register. There is no direct synchronisation between sender and receiver (e.g. DPLL or clock signal). Instead, each independently uses a locally generated copy of the clock set to the nominal baud rate. If the last two (stop) bits are not both set to one, then the slot is discarded.



Asynchronous transmission and reception using an 11-bit shift register.

The waveform should show the following for the A channel:

1) An idle period before the start - at the Mark level,
2) A start bit of one baud period at the space level.
3) A byte, represented in binary and alligned so it is lsb first - i.e. SMMM SSSS represents (0x0E)
4) Two bauds with a Mark value (the stop bit)

The answer must also show the balanced version of the waveform (inverted) on the B channel.

The answer should label the vertical axis (volts) and horizontal axis (time, in bauds or seconds).

1(b) 4 If the transmission baud rate is 250 kbps, what is the minimum duration of each slot?

4μS pulses (250 kbaud) with 8 data bits/slot. There is one start and two stop bits (parity is not used). The total slot duration for 11 bits is therefore 44 μS. For full marks students MUST explain working.

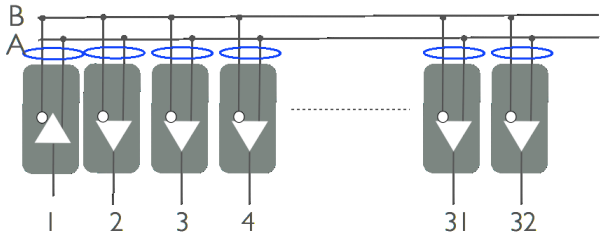
1(c) 8 How does a DMX-enabled fixture identify the start of a DMX-512 frame and thus determine the set of slots that it needs to receive?

The start of each DMX frame is therefore prefixed by a "break" signal, followed by a single control slot (usu. with a value zero). A receiver finds the start of frame, by listening for a break, followed by a Mark-After-Break (MAB) signal. In DMX, the break is 92 μS of continuous low (longer than a valid all zero slot) followed by a 12 μS high level (Mark After Break).

The first slot identifies the control value. This is zero for simple applications.

The remaining slots are identified by their position in a frame. Following this, each slot is asynchronously framed, starting with slot 1, then slot 2, etc.. The final slot is indicated by a long idle period after the slot. The Frame to frame period must be in the range1240 µS - 1S. This determines the maximum information rate over the bus.

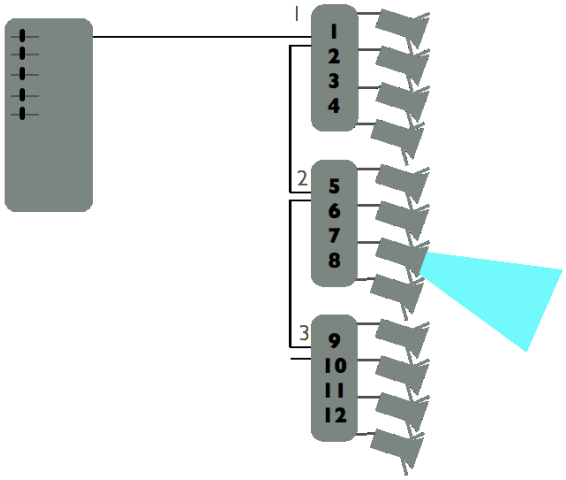
The usual application is to demultiplex the signal using up to 32 receivers per bus (more may be used if the signal is split into multiple busses). Each receiver decodes a set of slots from the frame.



Reception of DMX frames over the differential bus.

Each fixture is assigned a base address (a 9 bit binary number), often using a bank of DIP switches or a front panel to a microprocessor. The base address is fixed. More than one fixture may have the same base address, if they perform an identical interpretation of the control data (e.g. the same type of fixture) and they do not need to be independently controlled. The address determines the first slot that is used by the receiving device. Here are some examples:

- A device that uses four channels and has a base address of 1 will interpret the slots 1,2,3 and 4 to control its output values.
- A device that uses two channels and has a base address of 6 will ignore (skip) the first 5 slots (1-5) and will receive the slots 6 and 7.

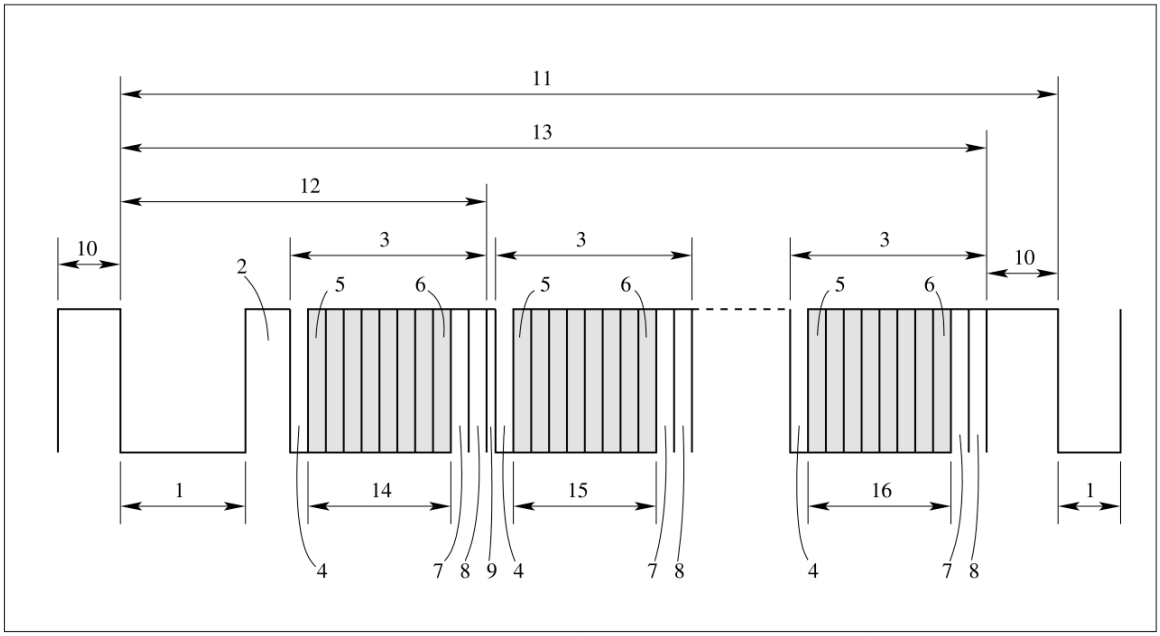


Demultiplexing to 3 4-channel dimmer packs, respectively slots 1-4, 5-8 and 9-12.

Q Marks

A receiver ***skips a number of bytes*** corresponding to the allocated base address. e.g. for address 8 skips 8 bytes. It then extracts a set of contiguous bytes (slots) from the DMX frame. Fixtures may use one slot or many, depending on the configuration - which must be consistent between the sender and receiver. The answer must clearly show each slot is associated with a channel and therefore that a receiver reacts to a pre-defined subset (group) of slots.

Answers to this question may utilise the following diagram, or a simplified version of this:



1. SPACE for BREAK
2. MARK after BREAK (MAB)
3. Slot Time
4. START bit
5. LEAST SIGNIFICANT Data BIT (LSB)
6. MOST SIGNIFICANT Data BIT (MSB)
7. STOP Bit
8. STOP bit
9. MARK time between slots
10. MARK before BREAK (MBB)
11. BREAK to BREAK time
12. RESET Sequence (BREAK, MAB, START Code)
13. DMX512 Packet
14. START CODE (SLOT 0 Data)
15. SLOT 1 Data
16. SLOT n DATA (Max. 512)

1d 5 A DMX fixture controls the output power supplied to a mains lamp. Sketch the waveform waveform for the voltage across the lamp for a slot value of 26 and 100.

The answer for the microcontroller output should show a square wave (e.g. +5V and 0V) with a frequency of 100 Hz (since this corresponds to the half-cycle time of the 50 Hz mains).

Phase modulation is provided by modulating the square wave using PWM based on the slot value assigned to the channel. An important feature is that the PWM output is synchronised, so that the trailing edge is just before the zero-crossing point of the mains cycle for the phase being dimmed.

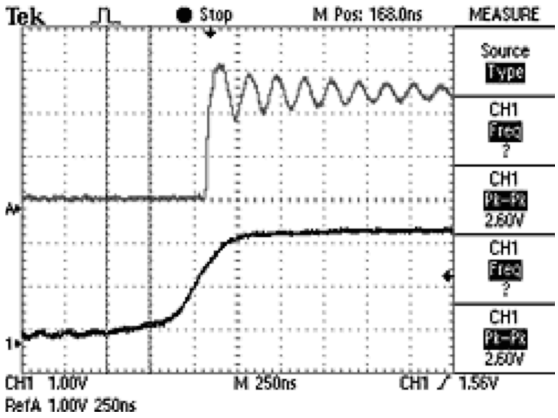
A slot value of 25/255 is approximately 10% of the cycle period. A value of 64/255 is 100 is just less than half a cycle.

In normal operation, the PWM waveform is use to fire a TRIAC (via the appropriate driver circuit). This results in an AC signal through the lamp that is turned on for the appropriate proportion of the last part of the mains half-cycle. This waveform is symmetric about 0V.

2.

(a) Why is the Slew Rate important when specifying the line driver to be used in a circuit? [4 marks]

Slew-rate limiting at the transmitter works by slowing the edges of the RS-485 signal down and therefore reducing the signal's high-frequency components An appropriate choice of driver/receiver circuit at the transmitter/receiver hence reduces radiated emissions and reduces susceptibility to noise and improper termination.



Time domain plots from an oscilloscope showing the start of a pulse sent with slew-rate limiting at 2.5 Mbaud (above) and one shaped to 250 kbaud (below).

A receiver circuit that supports a higher baud rate will be designed to accept a wider bandwidth input signal, this makes the receiver more susceptible to interference at higher frequencies and more vulnerable to noise.

(b) Why is a bias circuit needed for the Remote Device Management (RDM) protocol? [2 marks]

Needed because the protocol is half duplex, which means the controller sometimes enters high impedance mode (when listening for a response). The bias prevents the lines from floating to an arbitrary value that could result in receivers mis-interpreting the bus state.

(c) Calculate suitable component values for the bias circuit, given that RDM uses a cable with a nominal impedance of 120 Ohms. [5 marks]

Each RS-485 node has an input impedance of 12K.
32 nodes in parallel present load of 376 ohms.
Two 120 Ohm terminations add 60 Ohm load.
Total load is therefore 51.8 ohms.
To maintain at least 245 mV between B A line, needs a bias current of ~ 4.7 mA to flow through this load.
A 5V supply needs a series resistance of 1063 Ohms, subtract 51.8 Ohms from terminators, this leaves 1011 Ohms.
Placing half as a pull-up to 5V and half as a pull-down to ground gives a bias of 505 Ohms, 510 Ohms to nearest preferred value.

The RDM spec says “The command port shall provide a means to bias the termination of the data link to a value of at least 245 mV”

1/(0.0167+0.0026)=51.8

(d) Suggest some advantages to using RDM compared to DMX. [4 marks]

One advantage is that devices can be addressed by UID, which means devices do not have to be manually configured by DIP switches.
Devices can also return status information (e.g. temperature measurement, or no. of hours of operation).
A controller can configure a device remotely (e.g. to enable a specific profile).
A controller can determine all the devices connected to a bus.

Q Marks

(e) 10 Provide a set of diagrams and detailed explanation on <u>one</u> of the following topics, either:

How a controller using the RDM protocol may identify the nodes connected to the bus.

Master must discover UID of each device on network.
RDM allows device to be discovered by polling (binary search)
Do any devices have first bit set in UID?
Do these devices also have next bit set, etc?
Finally, one device found, and told to be quiet, loop repeats
- The algorithm may be sketched.
- A full answer may mention details, such as the binary search method and how to optimise this when some of the UIDs are provisionally known (e.g. from a previous discovery).

OR *or*

How a micro-controller may be programmed to receive a particular set of DMX data slots at a specified offset within a frame.

Pseudo-C for a receiver:

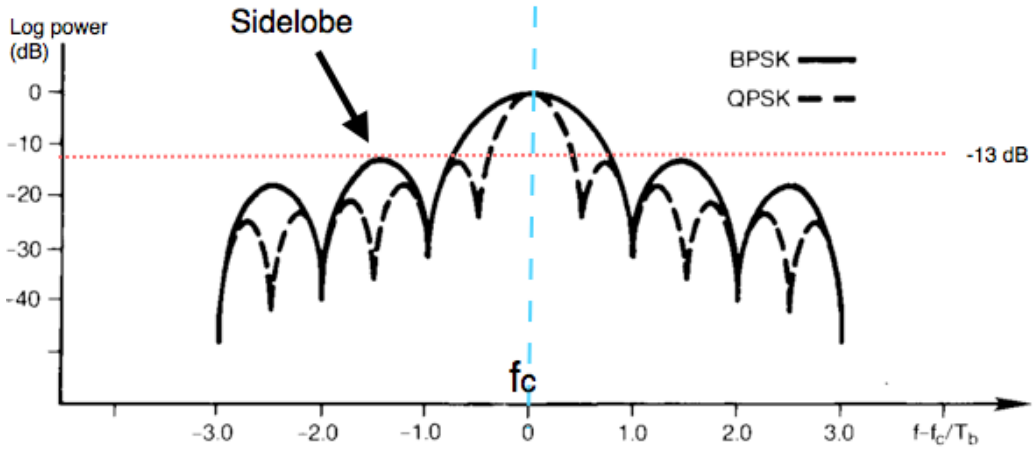
```
ISR (UART_RX_vect)
{
static  uint16_t DmxCount;
        uint8_t  USARTstate= UCSRA;       //get state before data!
        uint8_t  DmxByte   = UDR;         //get data
        uint8_t  DmxState  = gDmxState;   //load once to increase speed

if (USARTstate &(1<<FE))                  //check for break

   UCSRA &= ~(1<<FE);                     //reset flag
   DmxCount =  DmxAddress;                //reset slots counter
                                 //(count slots before start address)
   gDmxState= BREAK;
   }
else if (DmxState == BREAK)
   {
   if (DmxByte == 0) gDmxState= STARTB;  //normal start code detected
   else              gDmxState= IDLE;
   }
else if (DmxState == STARTB)
   {
   if (--DmxCount == 0)                   //start address reached?
        {
        DmxCount= 1;                      //set up counter for
                                          // required slots
        DmxRxField[0]= DmxByte;           //get 1st DMX channel of device
        gDmxState= STARTADR;
        }
   }
else if (DmxState == STARTADR)
   {
   DmxRxField[DmxCount++]= DmxByte;       //get channel
   if (DmxCount >= sizeof(DmxRxField))    //all slots received for device?
        {
        gDmxState= IDLE;                  //wait for next break
        }
   }
}
```

Equivalent state diagram or flow chart is also acceptable. All variables need to be explained.

Students are required to only answer (i) or (ii)

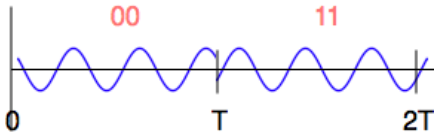
3(a) 6 Describe the use of *Quadrature Phase Shift Keying (QPSK)* to modulate data. Your answer must include appropriate diagrams to show the result of sending {00, 11}.

The sketch below may also be used, but is not required:



Note: vertical axis is in dB (logarithmic), should identify carrier frequency at centre
Could compare with BPSK (not required).

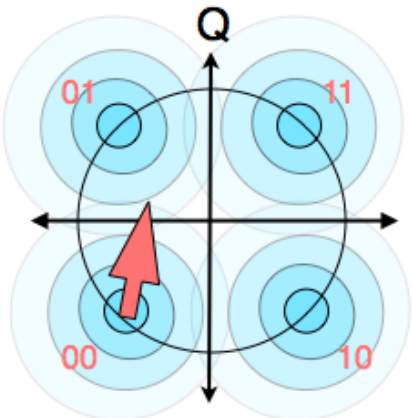
Example showing phase change when sending 00,11:



3**(b) 5 Use a constellation diagram to explain how errors may be introduced during demodulation, and why Gray Coding is used to encode the symbols.**

Answers should show a constellation diagram. The constellation diagram shows I and Q, and for QPSK have a 45 degree rotation. Answer may include such QPSK Constellation diagrams. When used over a link with noise, the "Bit patterns" overlap, increasingly more as the noise increases, resulting in ambiguity in demodulation. Usual ambiguity is small, and the use of Grey coding results in only one errored bit following a phase corruption.

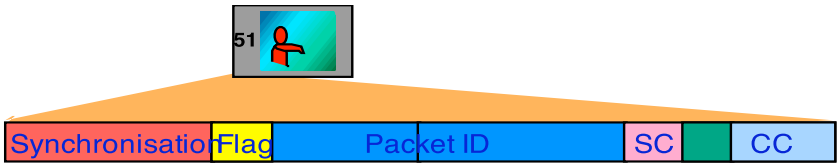
QPSK uses a symbol period of two bits and a phase change by 180 degrees at the symbol boundary:



3(c) **Use diagrams to explain the operation of *Time Division Multiplexing* in a *DVB Transport Stream*.** **[5 marks]**

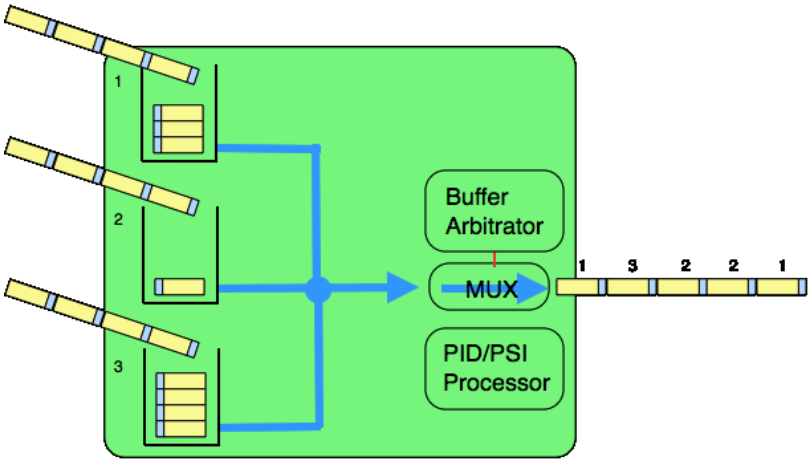
The transport stream is used to support a variety of different services. The basis of the Transport Stream is that all data to be sent is segmented into a ***fixed-sized*** Transport Stream (TS) Packet. Each TS Packet comprises 184 bytes of payload and a 4 byte packet header. (The TS relies on underlying FEC and modulation to guarantee a residual Bit Error Ratio (BER) better than 10-10.) The header of each TS Packet always starts with a well-known ***synchronisation byte*** (0x47 in hexadecimal, or its inverted value). Other parts of the header control the way the receiver process a TS Packet:

A set of flag bits follow the TS header sync byte to indicate how the payload should be processed. The first flag indicates whether there had been a transport error (i.e. the upstream link problem). The second flag indicates the start of a payload (payload_unit_start_indicator, PUSI). For video and audio streams, the PUSI indicates that the transport packet contains the start of a PES packet. This use is different when control data is sent in place of audio or video (i.e. "table sections" in MPEG-2 and DVB terminology, see later). The third flag is a priority indicator that may be used by TS multiplexers to prioritise TS Packets.



The 4 B MPEG-2 TS Packet Header

The following diagram (or similar) is expected, although the answer could describe this in words. The set of input streams (left) are ***multiplexed*** together (usually chosen so that all do not simultaneously transmit at their peak rates). A fixed-rate multiplexor follows a pre-assigned schedule, e.g. a 3-channel multiplexor could take one TS Packet from channel 1, two from channel 2, one from channel 3, etc. following a loop. This divides the output capacity in the ratio 25:50:25 between the input streams.



A 3-input TS Multiplexor

If the arrival rate of channel 1 exceeds 25% of the capacity and the other streams also have traffic a queue will form, until the input rate reduces and the backlog can be cleared. A more flexible approach could dynamically change the ratio depending on the backlog or pre-assigned rules using a buffer arbitrator. In such as case the aggregate bit rate can be substantially lower than the sum of the peak bit rate. The combined use of compression and multiplexing allows approximately 5 times the number of channels to be sent over a single satellite transponder.

To receive a particular programme, the receiver must first determine the Transport Multiplex (i.e. carrier frequency and bit rate of the MCPC multiplex). Once this is known, it must find the Transport Stream (and assigned PID) that was used to multiplex the particular required content. It can then filter the received stream of TS Packets to extract only those TS Packets that match the needed PID value.

3(d) 5 Explain how a *Transport Stream* maintains a constant bit rate, even when the aggregate bit rate from all the sources varies as a function of time.

The answer must show both understanding of the NULL packet to maintain the rate ***and*** the way in which the receiver identifies a NULL packet and silently discards it before other processing.

The sender inserts NULL TS packets whenever there is no data at the link layer of the sender or whenever the receive buffer of TS multiplexor under-runs.. A special (reserved) PID value (with all 13 bits set to 1, represented 0x1FFF in hexadecimal format) is used to indicate that there is no data to be sent. This is called a "NULL" TS Packet.

A receiver silently discards all NULL TS Packets. It also discards TS packets with an unknown PID, or one with a PID which is not required by the receiver, is simply discarded. In this way, the receiver sees a constant rate stream at the physical layer, but with variable rate after link-layer processing.

A statistical multiplexor will also delete NULL packets on reception, and re-insert appropriate sets of null packets to preserve the aggregate transmit rate.

3(e) The following *Transport Stream* packet is received:

```
47 40 10 1B 00 40 F0 2D 00 01 FD 00 00
F0 08 40 06 53 61 74 4C 61 62 F0 18 00 01
00 01 F0 12 44 0B 01 13 00 00 FF F1 03 06
90 00 0F 41 03 00 01 01 F9 03 DF BF FF FF
```

3(e) 2 (i) What is the purpose of the first byte of this packet?

This byte is the synchronisation alignment word. It denotes the start of a frame. Receivers scan the bit stream to find this value when looking for synch.

The byte is inverted every 8 frames to provide alignment of the FEC.

2 (ii) What is the PID value of the packet payload?

Locate the bytes in the TS header using chart provided, remove flags field.
The TS Header comprises: 47 40 10 1B

Q Marks

Synchronisation byte (8 bits) 0x47
Flags (3 bits) :
1.Transport error = 0
2.Start of a payload (payload_unit_start_indicator) = 1
3.Transport priority = 0
Packet Identifier (PID) (13 bits) = 0x010, or 16 in decimal
Scrambling control bits (2 bits) = 00
Adaption field control bits (2 bits) = 01
Continuity counter (4 bits) =0xB

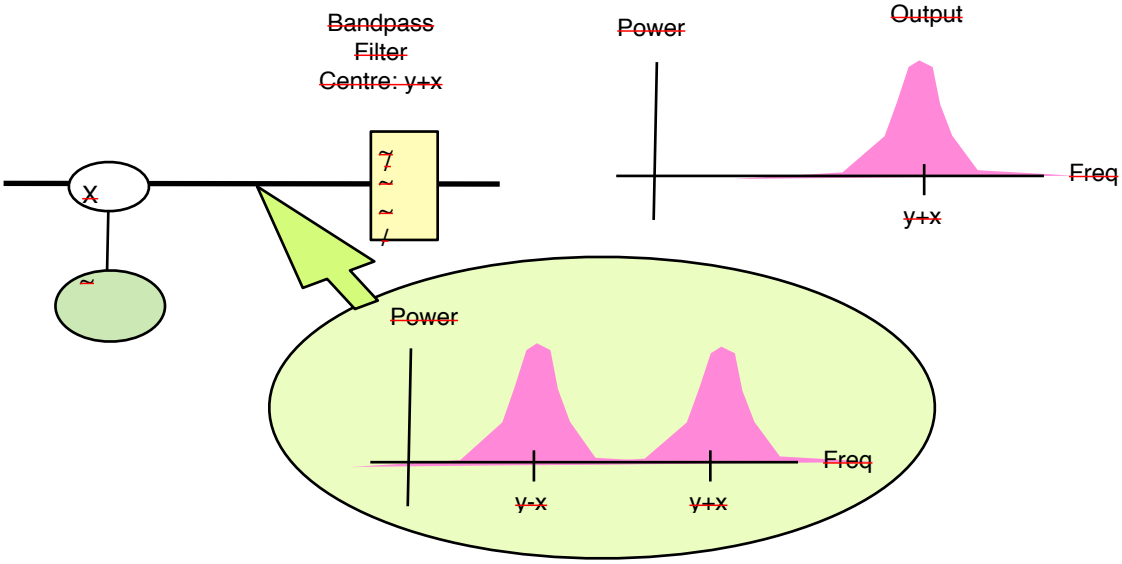
Hence, required answer is the PID has a value of 16, decimal.

4(a) 10 **The output signal from a satellite modem is often at an Intermediate Frequency (e.g. 70 MHz) and is later up-converted to a high-power microwave signal (e,g. 14 GHz) for transmission via the feed and antenna to the satellite. Describe how this up-conversion is performed. [10 marks]**

Answer should describe up-conversion

Mixer with LO & Filter (Image reject), IF amplifier. L.O. set to the offset in frequency replied. In this case, direct up-conversion to the satellite band would need the L.O. to be 14000 - 70 = 13.93 GHz. A two-stage up-conversion is also possible.

The up-conversion using the mixer generates both an upper and lower replica of the signal. Note the use of the bandpass filter after mixing to reject the unwanted (lower) product from mixing the LO and signal. There must also power amplification of the signal prior to transmission, this is usually done close to the dish to minimise losses before the signal leaves the terminal. A typical small terminal satellite system will use a 2W amplifier.



4(b) 5 **(A satellite terminal receives a signal at 11 GHz, and has an antenna diameter of 0.3 metres, what is the gain of this antenna? [5 marks]**

Antenna gain, G, measures the relative power received by an antenna, A, compared to sphere of 1m:

$G = \eta\pi^2D^2/\lambda^2$

η = Antenna efficiency, 0.35-0.8, typically 0.65
D = Diameter (2m)
$\lambda = 3 \times 10^8/f = 0.027$m

$G = 656$
$G = 10 \log(656) = 28$ dB

Q	Marks	
4(c)	10	**Provide a set of diagrams and detailed explanation on one of the following topics, either:**

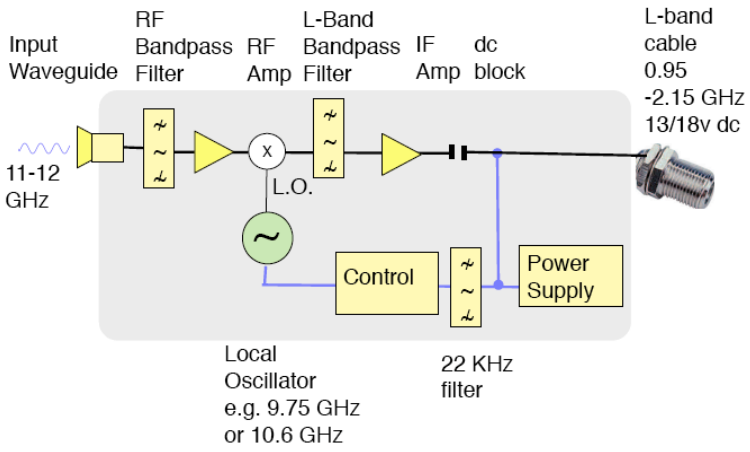
(i) To explain how a system generates a signal for transmission on the synchronous Controller Area Network (CAN) bus

CAN uses a differential 120 Ohm bus, in the same way as DMX and RDM. There are several key differences though:
- The bus is used synchronously, this requires zero-bit insertion for transparency and to regenerate the receive clock.
- There is no controller, this uses a method that enables the most important message to take control of the bus (overcoming regressive bits).
- Messages are short.
- Other salient features may be discussed. Suitable diagrams will be rewarded.

OR **(ii) To explain how a Low Noise Block (LNB) processes a DVB-S transmission prior to reception by a set top box.**

In a typical DVB-S receiver configuration, the feedhorn collects the microwave energy reflected by the antenna, and directs this to the receiving electronics that amplify and filter the signal, before block down-converting the signal from the satellite (at 11-12GHz) to an intermediate frequency at (approximately 1-2 GHz) using a mixer and a local oscillator. The resulting L-band (1-2 GHz) signal is amplified by the LNB for transmission down a 75 Ohm low-loss coaxial cable (e.g. CT-100) to the indoor DVB Receiver.

The diagram below shows a simplified Low Noise Block. Answer should explain how the microwave energy reflected by the satellite antenna is converted into an L-band signal and the role of each component:



Students are required to only answer (i) or (ii)